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10/709,718	05/24/2004	Ling-Yi Liu	IFTP0003USA	3717

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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,718	LIU ET AL.	
	Examiner	Art Unit	
	ERNEST UNELUS	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-44 and 83-109* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

3DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/20/09 has been entered.

Applicant's arguments filed 01/20/2009 with respect to claims 1-3, 5-11, 13-44, and 83-109 have been fully considered but are moot in view of the new ground(s) of rejection.

The rejection(s) of claim(s) 1-3, 5-11, 13-44, and 83-94 over Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Sebastian et al. (US pub. 2004/0083308) have been fully considered and is not persuasive. However, base on the amendment, the rejection has been withdrawn. Therefore, upon further consideration, a new ground(s) of rejection is made in view of Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and in further view of Nguyen (US pat. 7,146,521).

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. **Claims 1-3, 5-11, 13-44, and 83-109** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 6, 7, 10-22, 24-27, 29, 30, 32-53, 78-87, 90-93, and 97-103 of copending application No. 10/707,871 in view of Nguyen (US pat. 7,146,521).

3. Initially, it should be noted that the present application and Application No. 10/707,871, share one common inventor, which is Michael Schnapp. The assignee for both applications is Infortrend Technology, Inc.

4. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

5. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

6. Claim 1 is compared to claim 1 of application 10/707,871 in the following table:

Instant Application	**Application 10/707,871**
1. (currently amended) A computer system comprising: a host entity for issuing IO requests; an external **JBOD** emulation controller coupled to the host entity for emulating IO operations in response to the IO requests; and a group of physical storage devices (PSDs) coupled to the JBOD emulation controller each through a point-to-point serial-signal interconnect for providing storage to the computer system through the JBOD emulation controller, wherein	1. (currently amended) A storage virtualization computer system comprising: a host entity for issuing I0 requests; an external storage virtualization controller coupled to said host entity for executing I0 operations in response to said I0 requests; and a group of physical storage devices (PSDs) each coupled to the storage virtualization controller through a point-to-point serial-signal interconnect, for providing storage to the storage virtualization computer system through the storage virtualization controller;

said JBOD emulation controller defines at least one logical media unit (LMU) comprising sections of at said group of PSDs, and performs the following functions: **bringing the LMU on line while the JBOD emulation controller is on line, and taking the LMU off line while the JBOD emulation controller is on line**; and	
wherein said external JBOD emulation controller includes: a central processing circuitry for performing said IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to one of said PSDs	wherein said storage virtualization controller comprises: a central processing circuitry for performing said I0 operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to said host entity; and at least one device-side IO device interconnect port provided in one of said at least one I0 device interconnect controller for coupling to said group of PSDs through said point-to-point serial-signal interconnect, said device-side IO device interconnect port being a serial port for point-to-point serial-signal transmission; **wherein said computer system further comprises a detachable canister attached to said storage virtualization controller for containing one of said PSDs therein**; wherein said storage virtualization controller is configured to define at least one logical media unit consisting of sections of said group of PSDs; and wherein said SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying IO data into at

	least one data packet for transmission to said group of PSDs through said device-side IO device interconnect port: and wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission.

Claim 1 from the application 10/707,871 doesn't specifically discloses JBOD and a controller bringing the LMU on line while the JBOD emulation controller is on line, and taking the LMU off line while the JBOD emulation controller is on line.

Nguyen discloses use of a JBOD controller **(see col. 5, line 42, which discloses a JBOD system and col. 7, lines 55-56, which discloses, "In one embodiment, data storage operations are in accordance with the RAID-1 or RAID-5 protocol")** and wherein said JBOD emulation controller performs the following functions: bringing the LMU on line while the JBOD emulation controller is on line, and taking the LMU off line while the JBOD emulation controller is on line **(relying on the 'logical media unit' being an interface (144 of Bicknell) for the discs in the disc pack 118 of disc drive 106, see claim 1 of Nguyen, which discloses, "wherein the controller of each storage component is operable to: increase a fan speed if the controller detects a temperature of an overheating disk drive over a first**

threshold; remove the overheating disk drive from data storage operations if the controller detects the temperature of the overheating disk drive over a second threshold after the fan speed is increased, wherein the second threshold is greater than the first threshold; and temporarily activating the overheating drive so that data can be evacuated from the overheating disk drive to one or more properly functioning disk drives").

Application number 10/707,871 and Nguyen are analogous art because they are from the same field of endeavor of peripheral storage.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the computer system as taught by the instant application to include a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen.

The motivation for doing so would have been because Nguyen teaches, **"Overheating storage devices within the data storage system are detected, cooled, and removed from data transfer operations, and the data is evacuated to properly functioning components. Therefore, loss of data is avoided. Furthermore, when a problem is detected in a component, it can be placed offline before the problem is exacerbated with repeated data storage operations, perhaps extending the life of the component and of the entire system. In addition to the tremendous benefit of uninterrupted data storage with minimized risk of lost data, the serviceabilty of the data storage system is increased" (see col. 1, lines 48-58).**

Therefore, it would have been obvious to combine Nguyen (US pat. 7,146,521) with Applicant number 10/707,871 for the benefit of creating the computer system to obtain the invention as specified in claim 1.

This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The double patenting rejection is also applicable to other claims in the application; **for example**;

Constant Application	**Application 10/707,871**
(claim 2) The computer system of claim 1 wherein the point-to-point serial-signal interconnect is a Serial ATA IO device interconnect.	(claim 2) The storage virtualization computer system of claim 1 wherein said point-to-point serial-signal interconnect is a Serial ATA IO device interconnect.

And many others

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3, 5-9, 11, 13-17, 24-29, 31-35, 38-40, 44, 83, 84, 86-96, 98-100, 102, 103, 105-107, and 109**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and further in view of Nguyen (US pat. 7,146,521).

3. As per **claims 1, 8, and 11,** Bicknell discloses, "A computer system **(system 100 of fig. 6)** comprising:

a host entity **(Host computer of fig. 6)** for issuing IO requests;

an external JBOD emulation controller **(controller 1)** coupled to the host entity for emulating IO operations in response to the IO requests **(see fig. 6 and paragraph 0029) (see paragraph 0017 for emulation)**; and

a group of physical storage devices (PSDs) **(discs in the disc pack 118 of disc drive 106, as discloses in paragraph 0018; see also figs. 3 and 6)** coupled to the JBOD emulation controller each through a point-to-point serial-signal interconnect **(see fig. 6 and paragraph 0019)** for providing storage to the computer system through the JBOD emulation controller **(see paragraph 0027)**, wherein

said JBOD emulation controller defines at least one logical media unit (LMU) **(the data interface 144 of fig. 6)** comprising sections of said group of PSDs **(see fig. 3 or 6, which discloses the interface as part of the disc drives)**;

but fails to disclose expressly "wherein said external JBOD emulation controller includes: a central processing circuitry for performing said IO operations in response to IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to one of said PSDs".

Meehan discloses wherein said external JBOD emulation controller includes: a central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for performing said IO operations in response to IO requests of said host entity **(see fig. 5 and para. 0028)**;

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para. 0028)** coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **(interface connector 410 of fig. 6)** provided in a said at least one IO device interconnect controller for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage disks 401-404 would move from the host interface 411 (from the host), optionally through a primary RAID Controller (if present), through the Interface connector 410, and into the buffer RAM 407 of RAID Controller 400")**; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to one of said PSDs **(see para. 0029, which discloses "For example, data may be transmitted between the RAID controllers and storage devices by means of an SCA or other type Interface Connector 410". See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect)**.

Neither Bicknell nor Meehan specifically discloses a RAID controller being use as JBOD controller and wherein said JBOD emulation controller performs the following functions: bringing the LMU on line while the JBOD emulation controller is on line, and taking the LMU off line while the JBOD emulation controller is on line.

Nguyen discloses a RAID controller being use as JBOD controller **(see col. 5, line 42, which discloses a JBOD system and col. 7, lines 55-56, which discloses, "In one embodiment, data storage operations are in accordance with the RAID-1 or RAID-5 protocol")** and wherein said JBOD emulation controller performs the following functions: bringing the LMU on line while the JBOD emulation controller is on line, and taking the LMU off line while the JBOD emulation controller is on line **(relying on the 'logical media unit' being an interface (144 of Bicknell) for the discs in the disc pack 118 of disc drive 106, see claim 1 of Nguyen, which discloses, "wherein the controller of each storage component is operable to: increase a fan speed if the controller detects a temperature of an overheating disk drive over a first threshold; remove the overheating disk drive from data storage operations if the controller detects the temperature of the overheating disk drive over a second threshold after the fan speed is increased, wherein the second threshold is greater than the first threshold; and temporarily activating the overheating drive so that data can be evacuated from the overheating disk drive to one or more properly functioning disk drives").**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Nguyen (US pat. 7,146,521) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more

specifically, to a multiple level RAID architecture as taught by Meehan, and a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen.

The motivation for doing so would have been because Meehan teaches that, **"In addition, a RAID 0 stripe can be written to the storage devices at the same time. This stripe allows for the data to be evenly written to the devices 120 in an attempt to maximize overall system performance" (see paragraph 0006), and Nguyen teaches, "Overheating storage devices within the data storage system are detected, cooled, and removed from data transfer operations, and the data is evacuated to properly functioning components. Therefore, loss of data is avoided. Furthermore, when a problem is detected in a component, it can be placed offline before the problem is exacerbated with repeated data storage operations, perhaps extending the life of the component and of the entire system. In addition to the tremendous benefit of uninterrupted data storage with minimized risk of lost data, the serviceabilty of the data storage system is increased" (see col. 1, lines 48-58).**

Therefore, it would have been obvious to combine Nguyen (US pat. 7,146,521), Meehan et al. (US pub. 2004/0177218), and Bicknell et al. (US pub. 2003/0193776) for the benefit of creating the computer system to obtain the invention as specified in claims 1, 8, and 11.

4. As per **claims 2, 9, 84, and 93**, the combination of Bicknell, Meehan, and Nguyen disclose "The computer system of claim 1" **[See rejection to claim 1 above]**, Bicknell further

discloses wherein the point-to-point serial-signal interconnect is a Serial ATA IO device interconnect **(see fig. 6 and paragraph 0019).**

5. As per **claims 3, 10, 41, 43, 85, and 94**, the combination of Bicknell, Meehan, and Nguyen disclose "The computer system of claim 1" **[See rejection to claim 1 above]**, Meehan further discloses wherein the point-to-point serial-signal interconnect is a Serial-Attached (SAS) IO device interconnect **(see paragraph 0029).**

6. As per **claim 5**, the combination of Bicknell, Meehan, and Nguyen disclose "The computer system of claim 1" **[See rejection to claim 1 above]**, Bicknell further discloses wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port **(see paragraph 0019, which disclose a redundancy system)**.

7. As per **claim 6,** the combination of Bicknell, Meehan, and Nguyen disclose "The computer system of claim 1" **[See rejection to claim 1 above]**, comprises a second external JBOD emulation controller **(controller 2 of fig. 6)** coupled to the host entity for emulating IO operations in response to the IO requests **(see fig. 6 and paragraph 0029)**, wherein said external JBOD emulation controller and said second external JBOD emulation controller are configured into a redundant pair **(see paragraph 0019)**, and said LMU is allowed to be brought on line or taken off line while the JBOD emulation controller is on line **(see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of**

subsystem 100"; therefore, when the disc drive does off line, since the interface is part of it, it will also goes off line).

8. As per **claim 7**, the combination of Bicknell, Meehan, and Nguyen disclose "The computer system of claim 6" **[See rejection to claim 6 above]**, Bicknell further discloses wherein said LMU can be redundantly presented to the host by both of said external JBOD emulation controllers **(see paragraph 0037).**

9. As per **claims 13, 86, and 89,** the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Nguyen further discloses, comprises auto-on-lining mechanism to automatically bring on line one of said LMU which was previously off-line once a requisite quorum of said PSDs comes on-line **(see claim 1 of Nguyen).**

10. As per **claims 14, 87, and 90,** the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Nguyen further discloses, comprises auto-off-lining mechanism to automatically take off line one of said LMU which was previously on-line once a requisite quorum of said PSDs becomes off-line **(see claim 1 of Nguyen)**.

11. As per **claim 15,** the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses, comprises

determining mechanism for automatically determining when one of said PSDs has been removed or when one has been inserted **(see paragraph 0019).**

12. As per **claim 16,** the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses, comprising scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSDs **(see paragraph 003, which discloses noticing a connection, which is a form of scanning)**.

13. As per **claim 17,** the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses, comprising informing mechanism for informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed **(see paragraph 0017, which disclose changed of mapping)**.

14. As per **claim 24**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein a first and a second of said at least one JBOD emulation controller are configured into a redundant pair, whereby when the first JBOD emulation controller goes off line or is taken off line, the second JBOD emulation controller will take over the functionality of the first JBOD emulation controller **(see paragraph 0017).**

15. As per **claim 25**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 24" **[See rejection to claim 24 above]**, Bicknell further discloses wherein a

host-side port of said first JBOD emulation controller and a host-side port of said second JBOD emulation controller are configured into a complementary port pair **(see paragraph 0017).**

16. As per **claim 26**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 25" **[See rejection to claim 25 above]**, Bicknell further discloses wherein said complementary port pair are interconnected onto a same host-side IO device interconnect **(see fig. 6, which discloses one host computer)**

17. As per **claim 27**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 26" **[See rejection to claim 26 above]**, Bicknell further discloses wherein said complementary port pair are interconnected together with switch circuitry **(see midplane card 112 of fig. 6).**

18. As per **claim 28**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 25" **[See rejection to claim 25 above]**, Bicknell further discloses wherein each port of said complementary port pair is interconnected onto a different host-side IO device interconnect **(see fig. 6).**

19. As per **claim 29**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 24" **[See rejection to claim 24 above]**, Bicknell further discloses wherein a said LMU is presented to the host entity through both said first and said second JBOD emulation controllers **(see fig. 6).**

20. As per **claim 31**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port **(see fig. 6 and paragraph 0037).**

21. As per **claims 32, 98, 105, and 109**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" [**See rejection to claim 8 above**], Bicknell further discloses wherein comprising an enclosure management services (EMS) mechanism [**(MUX 208 of fig. 8), in regards to an "enclosure management service", the applicant discloses "*Yet another feature of a JBOD subsystem is enclosure management services (EMS). This is an intelligent circuitry that monitors status of various enclosure devices, such as power supplies, fans, temperatures, etc.* Similarly, Bicknell discloses "The multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220)"see paragraph 0037. The electronics connection, as discloses, is power supplies**].

22. As per **claim 33**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 32" **[See rejection to claim 32 above]**, Bicknell further discloses wherein said EMS mechanism is of a direct-connect EMS configuration **(see fig. 8)**.

23. As per **claim 34**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 32" **[See rejection to claim 32 above]**, Bicknell further discloses wherein said EMS mechanism is of a device-forward EMS configuration **(see fig. 8)**.

24. As per **claim 35**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 32" **[See rejection to claim 32 above]**, Bicknell further discloses wherein said EMS mechanism implements both direct-connect and device-forward EMS configurations **(see fig. 8)**.

25. As per **claim 38**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode **(see paragraph 0030 and fig. 6)**.

26. As per **claim 39 and 91**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode **(see paragraph 0032 and fig. 6)**.

27. As per **claim 40**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein at

least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode **(see paragraph 0030 and fig. 6)**.

28. As per **claim 44**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell further discloses wherein at least one said host-side IO device interconnect port is Serial ATA operating in target mode **(see paragraph 0019).**

29. As per **claims 83, 88, and 92**, Bicknell discloses "A method **(system 100 of fig. 6)** for performing JBOD emulation in a computer system having at least one external JBOD emulation controller **(controller 1 of fig. 6) (see paragraph 0017 for emulation)** and a group of physical storage devices (PSDs) **(discs in the disc pack 118 of disc drive 106, as discloses in paragraph 0018; see also figs. 3 and 6)** connected to the JBOD emulation controller **(see fig. 6)**, the method comprising: defining at least one logical media unit (LMU) **(the data interface 144 of fig. 6)** comprising sections of said group of PSDs **(see fig. 3 or 6, which discloses the interface as part of the disc drives)** by the JBOD emulation controller; receiving and parsing IO requests from a host entity by the JBOD emulation controller to perform an IO operation to access the LMU by accessing said group of PSDs through at least one device-side IO device interconnect port in point-to-point serial signal transmission **(see fig. 6 and paragraph 0019)**;

but fails to disclose expressly "wherein said external JBOD emulation controller includes: a central processing circuitry for performing said IO operations in response to IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said PSDs".

Meehan discloses wherein said external JBOD emulation controller includes: a central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for performing said IO operations in response to IO requests of said host entity **(see fig. 5 and para. 0028)**;

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para. 0028)** coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **(interface connector 410 of fig. 6)** provided in a said at least one IO device interconnect controller for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage disks 401-404 would move from the host interface 411 (from the host), optionally through a primary RAID Controller (if present), through the Interface connector 410, and into the buffer RAM 407 of RAID Controller 400")**; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said PSDs **(see para. 0029, which discloses "For example, data may be transmitted between the RAID controllers and storage devices by means of an SCA or other type Interface Connector 410". See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect)**.

Neither Bicknell nor Meehan specifically discloses a RAID controller being use as JBOD controller and wherein said JBOD emulation controller performing the following functions: while the JBOD emulation controller is on line, bringing on line one of said at least one logical media unit which is not on line, and while the JBOD emulator controller is on line, taking off line one of said at least one logical media unit which is on line.

Nguyen discloses a a RAID controller being use as JBOD controller **(see col. 5, line 42, which discloses a JBOD system and col. 7, lines 55-56, which discloses, "In one embodiment, data storage operations are in accordance with the RAID-1 or RAID-5 protocol")** and wherein said JBOD emulation controller performing the following functions: while the JBOD emulation controller is on line, bringing on line one of said at least one logical media unit which is not on line, and while the JBOD emulator controller is on line, taking off line one of said at least one logical media unit which is on line **(relying on the 'logical media unit' being an interface (144 of Bicknell) for the discs in the disc pack 118 of disc drive 106, see claim 1 of Nguyen, which discloses, "wherein the controller of each storage component is operable to: increase a fan speed if the controller detects a temperature of an overheating disk drive over a first threshold; remove the overheating disk drive from data storage operations if the controller detects the temperature of the overheating disk drive over a second threshold after the fan speed is increased, wherein the second threshold is greater than the first threshold; and temporarily activating the overheating drive so that data can be evacuated from the overheating disk drive to one or more properly functioning disk drives").**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Nguyen (US pat. 7,146,521) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen.

The motivation for doing so would have been because Meehan teaches that, **"In addition, a RAID 0 stripe can be written to the storage devices at the same time. This stripe allows for the data to be evenly written to the devices 120 in an attempt to maximize overall system performance" (see paragraph 0006), and Nguyen teaches, "Overheating storage devices within the data storage system are detected, cooled, and removed from data transfer operations, and the data is evacuated to properly functioning components. Therefore, loss of data is avoided. Furthermore, when a problem is detected in a component, it can be placed offline before the problem is exacerbated with repeated data storage operations, perhaps extending the life of the component and of the entire system.**

In addition to the tremendous benefit of uninterrupted data storage with minimized risk of lost data, the serviceabilty of the data storage system is increased" (see col. 1, lines 48-58).

Therefore, it would have been obvious to combine Nguyen (US pat. 7,146,521), Meehan et al. (US pub. 2004/0177218), and Bicknell et al. (US pub. 2003/0193776) for the benefit of creating the computer system to obtain the invention as specified in claims 83, 88, and 92.

29. As per **claims 95, 99, 102, and 106**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Nguyen further discloses wherein said external JBOD emulation controller is adapted for accommodating said group of PSDs of different serial protocols **(see col. 7, lines 55-58)**.

30. As per **claims 96, 100, 103, and 107**, the combination of Bicknell, Meehan, and Nguyen disclose "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, Bicknell discloses wherein said group of PSDs are received in a plurality of enclosures (see figs. 3 and 6).

31. **Claims 36 and 37**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Nguyen (US pat. 7,146,521) as applied to claim 32, and further in view of Rabinovitz et al. (US pat. 6,483,107).

32. As per **claim 36**, the combination of Bicknell, Meehan, and Nguyen discloses "The JBOD subsystem of claim 32," **[See rejection to claim 32 above]**, including the enclosure

management services mechanism **(MUX 208 of fig. 8, as Bicknell discloses)**, but fails to disclose expressly wherein said enclosure management services mechanism is configured to support SES enclosure management services protocol.

Rabinovitz discloses a SES in a storage virtualization subsystem **(col. 17, line 23).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Nguyen (US pat. 7,146,521), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen, and a canister and a casing of a computer peripheral enclosure as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SES allow a user to monitor the enclosure from a remote location **(see col. 17, lines 29-31).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107) with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and

Nguyen (US pat. 7,146,521) for the benefit of creating the storage virtualization subsystem to obtain the invention as specified in claims 36.

33. As per **claim 37**, the combination of Bicknell, Meehan, Nguyen, and Rabinovitz discloses "The JBOD subsystem of claim 32," **[See rejection to claim 32 above]** Bicknell discloses the enclosure management services mechanism, and Rabinivitz further discloses the SAF-TE, **(see col. 17, line 29).**

34. **Claims 18-23 and 30**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Nguyen (US pat. 7,146,521) as applied to claim 8, and further in view of Watanable (US pub. 2004/0260873).

35. As per **claim 18**, the combination of Bicknell, Meehan, and Nguyen discloses, "The JBOD subsystem of claim 8" **[See rejection to claim 8 above]**, including a plurality of physical storage devices **(see fig. 6 of Bickell)**, but fails to disclose expressly comprising unique ID determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem.

Watanable discloses comprising unique ID determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem **(see paragraph 0114).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Nguyen (US pat. 7,146,521), and Watanable (US pub. 2004/0260873) are analogous art because they are from the same field of endeavor of data transfer from a host to multiple storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen, and a system and method invention to enable primary storage data or secondary storage data to be replicated such that a loss of primary or secondary data due to a concurrent or other system error might be avoided as taught by Watanable.

The motivation for doing so would have been because Watanable teaches that, " **Management of the storage system on a per system group basis facilitates management as compared with per volume management, and further facilitates scripting of storage system management functions" (see paragraph 0115).**

Therefore, it would have been obvious to combine Watanable (US pub. 2004/0260873) with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Nguyen

(US pat. 7,146,521) for the benefit of creating the computer system to obtain the invention as specified in claim 18.

36. As per **claim 19**, the combination of Bicknell, Meehan, Nguyen, and Watanable discloses "The JBOD subsystem of claim 18," **[See rejection to claim 18 above]**, Watanable further discloses wherein information used to uniquely identify each of said PSDs is stored on said PSDs **(see paragraph 0114).**

37. As per **claim 20**, the combination of Bicknell, Meehan, Nguyen, and Watanable discloses "The JBOD subsystem of claim 8," **[See rejection to claim 8 above]**, Watanable further discloses wherein LMU identification and configuration information is stored on the member PSDs that compose the LMU **(see paragraph 0114).**

38. As per **claims 21 and 30**, the combination of Bicknell, Meehan, Nguyen, and Watanable discloses "The JBOD subsystem of claim 20," **[See rejection to claim 20 above]** Watanable further wherein LMU identification information presented to the host entity is generated from said LMU identification information stored on the member PSDs that compose the LMU **(see paragraph 0114).**

39. As per **claim 22**, the combination of Bicknell, Meehan, Nguyen, and Watanable discloses "The JBOD subsystem of claim 8," **[See rejection to claim 8 above]** Watanable further discloses wherein LMU identification information presented to the host entity is generated from

information stored in a non-volatile memory in the JBOD emulation controller **(see paragraphs 0065 and 0114).**

40. As per **claim 23**, the combination of Bicknell, Meehan, Nguyen, and Watanable discloses "The JBOD subsystem of claim 8," **[See rejection to claim 8 above]** Watanable further discloses wherein LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information off of the member PSDs and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible **(see paragraph 0094, which discloses the assignment of the Ids to the storage device. See also paragraphs 0065 and 0114).**

41. **Claim 42,** is rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Nguyen (US pat. 7,146,521) as applied to claim 9, and further in view of Colton (US pub. 2005/0089027).

42. As per **claim 42**, the combination of Bicknell, Meehan and Nguyen discloses, "The computer system of claim 9," **[See rejection to claim 9 above]**, including at least one said host-side IO device interconnect port **(see fig. 6 of Bickell)**, but fails to disclose expressly wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode.

Colton discloses ethernet supporting the iSCSI protocol operating in target mode **(see fig. 11 and paragraph 1487, which discloses internet SCSI in an Ethernet network).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Nguyen (US pat. 7,146,521), and Colton (US pub. 2005/0089027) are analogous art because they are from the same field of endeavor of data transfer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen, and a system and method for transferring data optically via an intelligent optical switching network as taught by Colton.

The motivation for doing so would have been because Colton teaches that **"The Sun server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance" (see paragraph 1487).**

Therefore, it would have been obvious to combine Colton (US pub. 2005/0089027) with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Nguyen

(US pat. 7,146,521) for the benefit of creating the computer system to obtain the invention as specified in claim 42.

43. **Claims 97, 101, 104, and 108**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Nguyen (US pat. 7,146,521) as applied to claim 1, and further in view of Rinaldis et al. (US pat. 7,107,343).

44. As per **claims 97, 101, 104, and 108**, the combination of Bicknell, Meehan, and Nguyen discloses, "The JBOD subsystem of claim 8" [**See rejection to claim 8 above**], Meehan and Nguyen further discloses wherein said external JBOD emulation controller **(a primary RAID controller, as illustrated in fig. 3 of Meehan)** issues a device-side IO request to said IO device interconnect controller **(a secondary RAID controller)**, and said IO device interconnect controller re-formats said device-side IO request and accompanying IO data into at least one data packet for transmission to said group of PSDs through said device-side IO device interconnect port **(see para. 0029 of Meehan, which discloses the FPGA 409 'manipulating' data between the host and the storage devices. Manipulating is a form of 're-formatting'. The claim language is not specific as to how this reformatting is being done. See also para. 0016, which discloses 're-distributed' the data).**

Neither Bicknell, Meehan, nor Nguyen discloses "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual I0 information to transmit through the SAS device-side I0 device interconnect port, and a check data segment

containing check codes derived from said payload for checking the correctness of said payload data after transmission".

Rinaldis discloses "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual I0 information to transmit through the SAS device-side I0 device interconnect port, and a check data segment containing check codes derived from said payload for checking the correctness of said payload data after transmission" **(see col. 6, lines 20-25)**.

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Nguyen (US pat. 7,146,521), and Rinaldis et al. (US pat. 7,107,343) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a data storage system and method capable of reducing the operating temperature of the data storage system, removing any overheating storage devices from operation, reconstructing data, and evacuating data from the overheating storage devices before the devices and the data are damaged or lost systems and techniques to synchronize network configuration for a hardware accelerated network protocol as taught by Nguyen, and a low cost system for providing improved RAID 1 performance as described Rinaldis.

The motivation for doing so would have been because Meehan teaches, "In addition, a RAID 0 stripe can be written to the storage devices at the same time. This stripe allows for the data to be evenly written to the devices 120 in an attempt to maximize overall system performance" (see paragraph 0006). See also col. 2, lines 44-46 of Rinaldis, which discloses "Accordingly, the present invention provides a RAID 1 controller that is capable of operating at higher speeds than conventional RAID 1 controllers".

Therefore, it would have been obvious to combine Rinaldis et al. (US pat. 7,107,343) with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Nguyen (US pat. 7,146,521) for the benefit of creating the computer system to obtain the invention as specified in claims 97, 101, 104, and 108.

V. RELEVANT ART CITED BY THE EXAMINER

1. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

2. The following reference teaches an external JBOD emulation controller coupled to a host peripheral storage devices

U.S. PATENT NUMBER

US 6,574,709; 7,107,320; 2002/0133735; 6,467,034

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-3, 5-11, 13-44, and 83-109 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

March 17, 2009
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